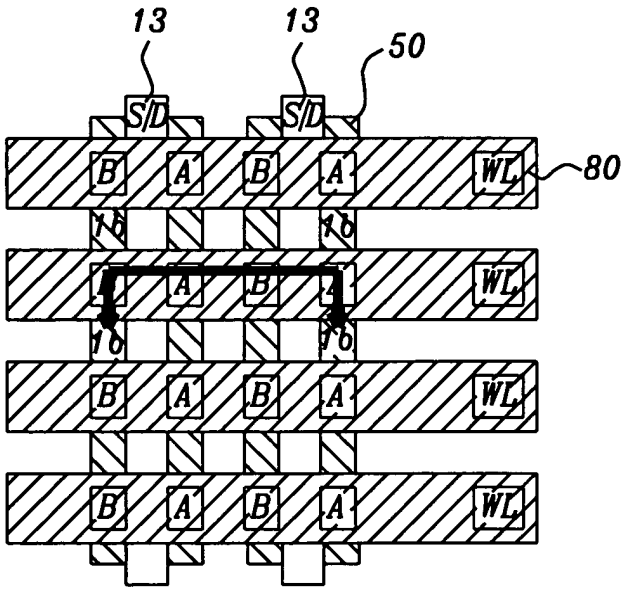


FIG. 1a – Prior Art

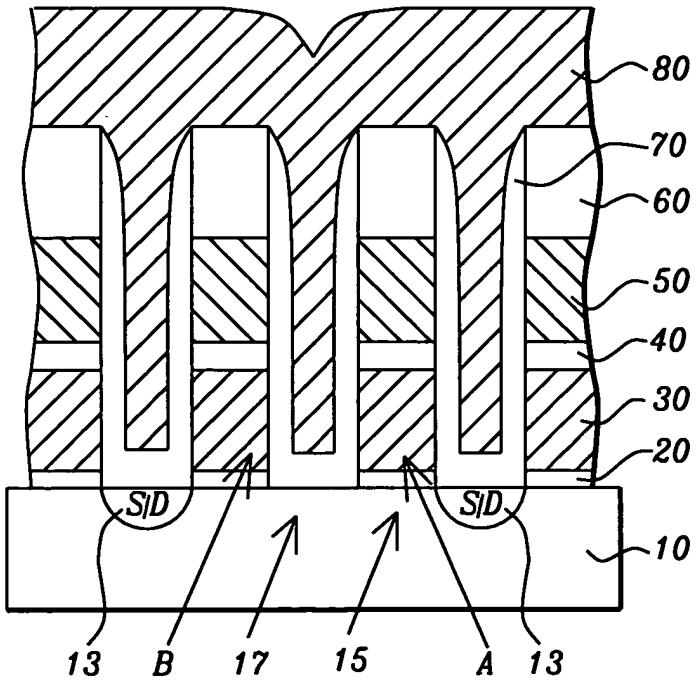


FIG. 1b – Prior Art

Table of Keys to Figures

D : drain as BIT LINE
S : source
CG: control gate
SG: selected gate as WORD LINE
TG: transfer gate

: seleceted cell

: un-selected cell

FIG. 1c – Prior Art

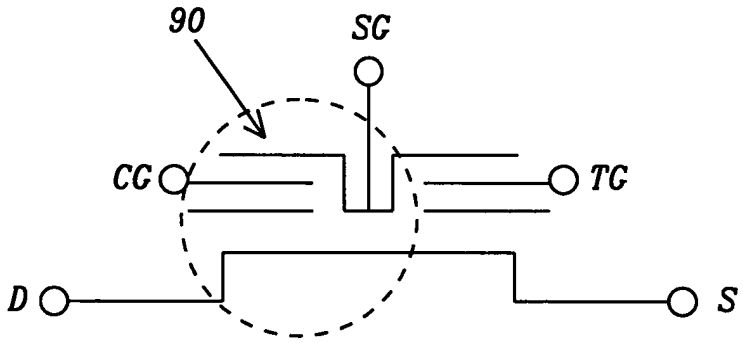


FIG. 1d – Prior Art

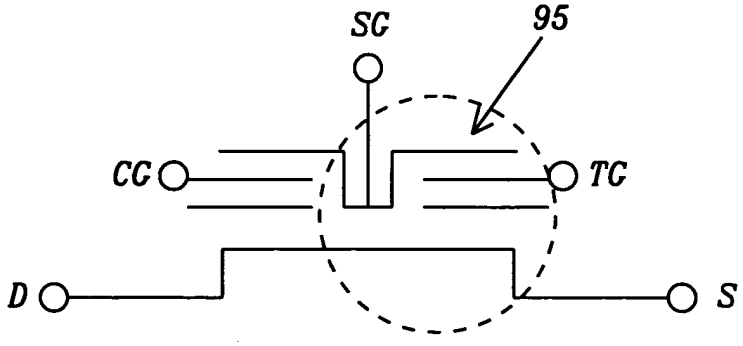


FIG. 1e – Prior Art

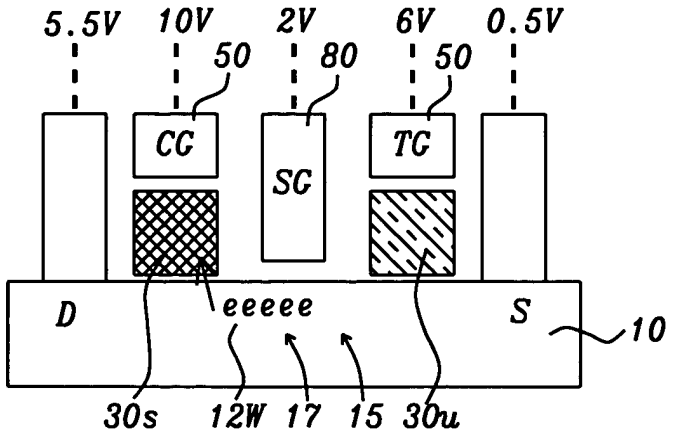


FIG. 2a – Prior Art

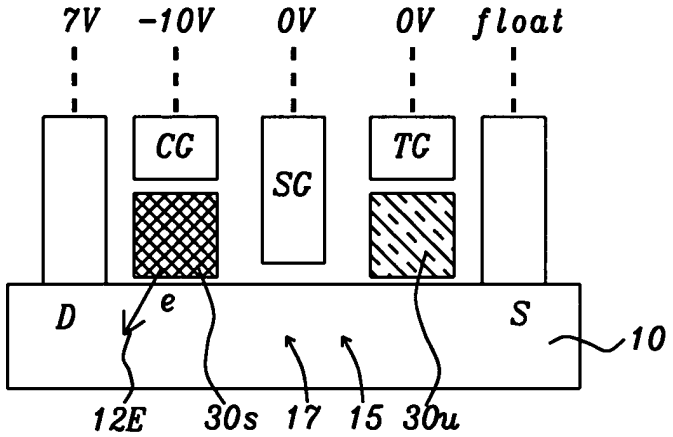


FIG. 2b – Prior Art

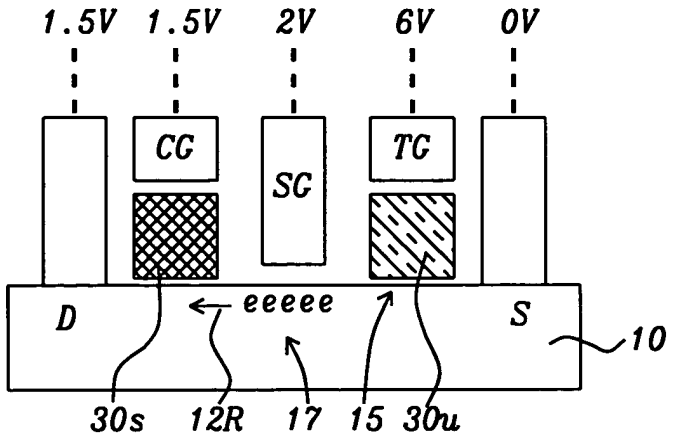


FIG. 2c – Prior Art

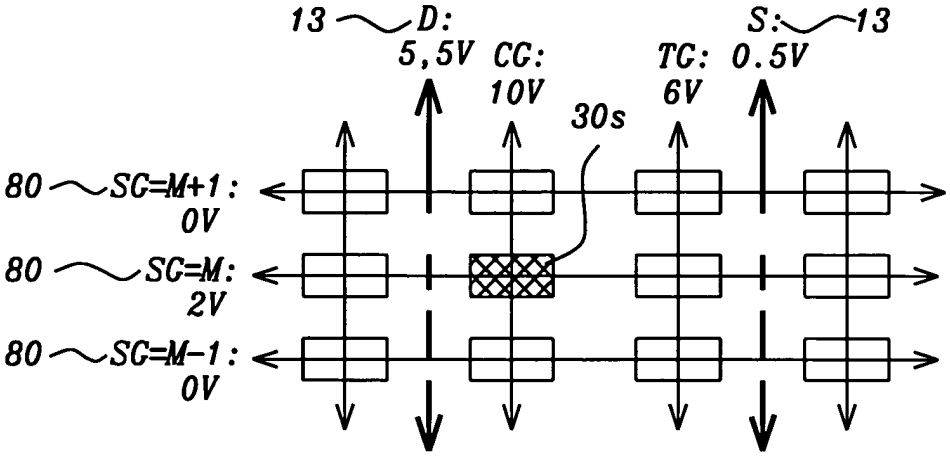


FIG. 3a – Prior Art

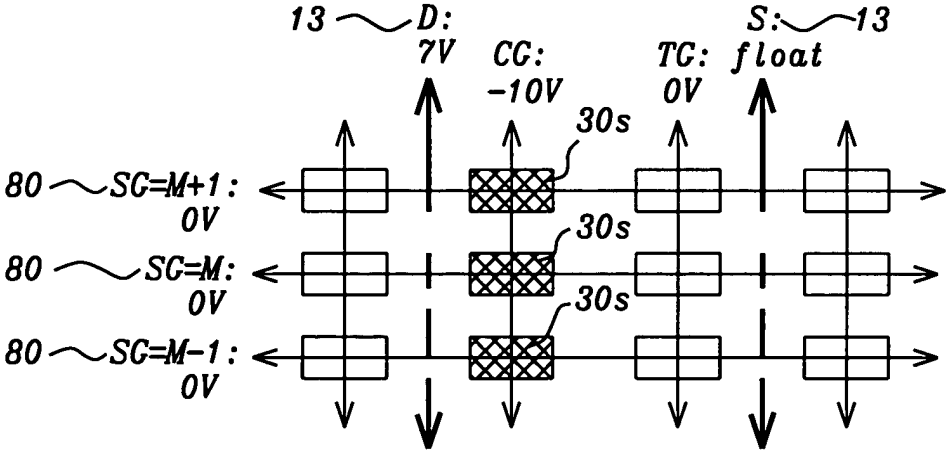


FIG. 3b – Prior Art

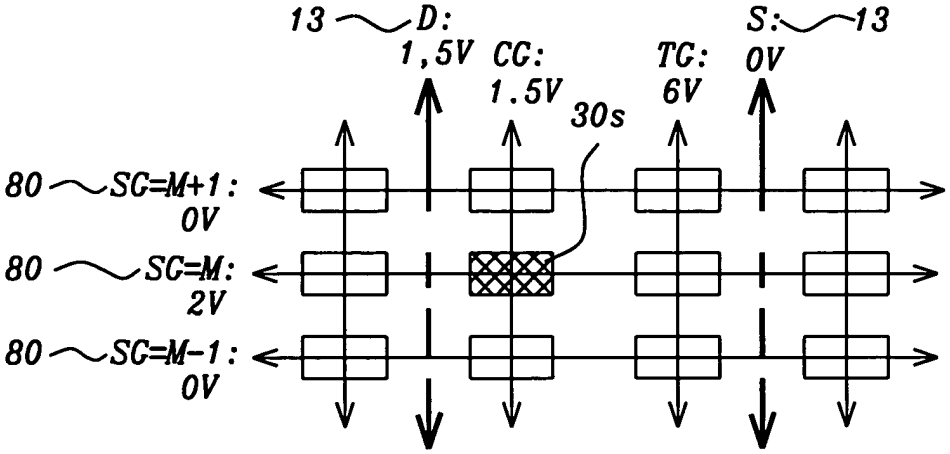


FIG. 3c – Prior Art

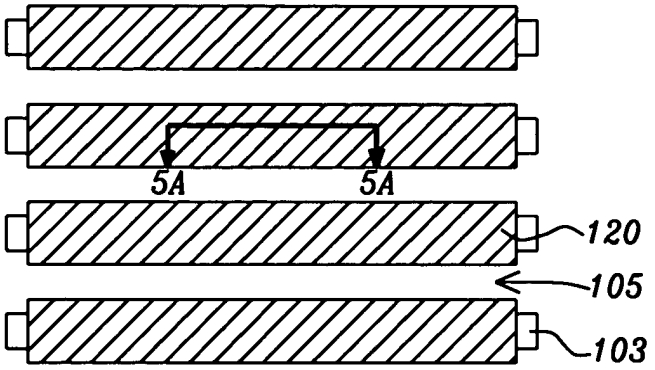


FIG. 4a

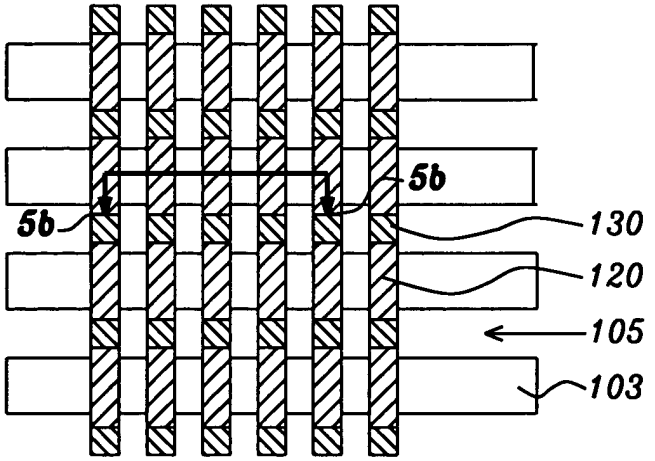


FIG. 4b

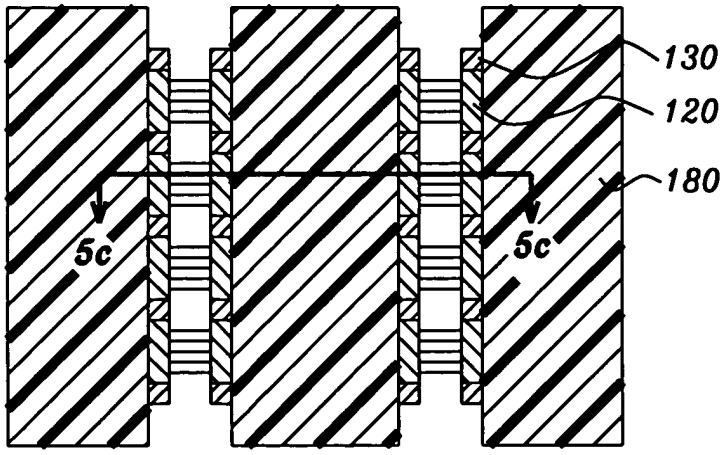


FIG. 4c

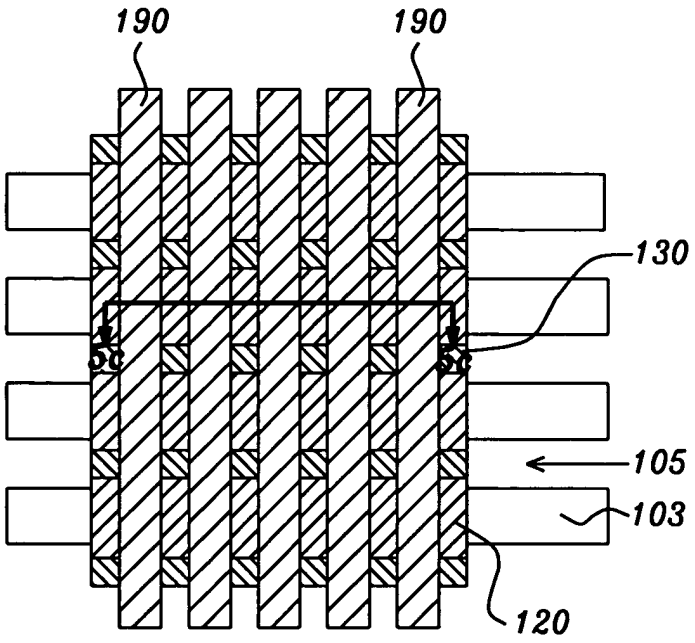


FIG. 4d

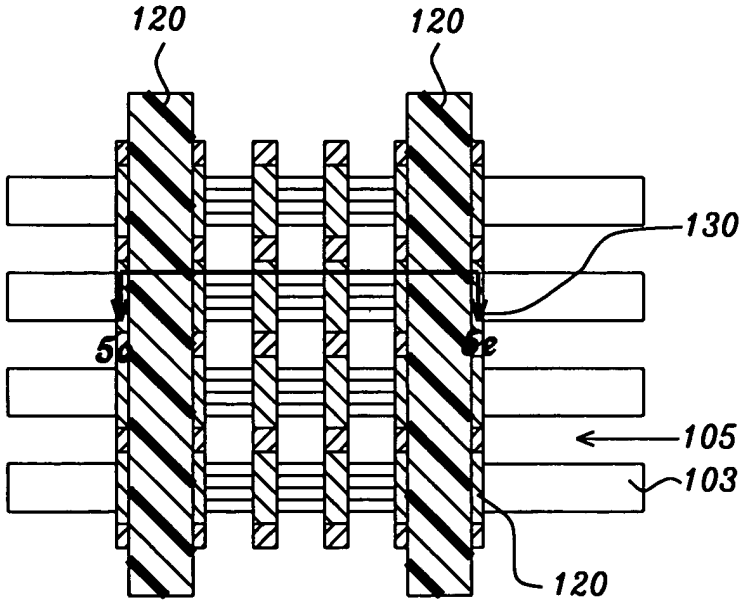


FIG. 4e

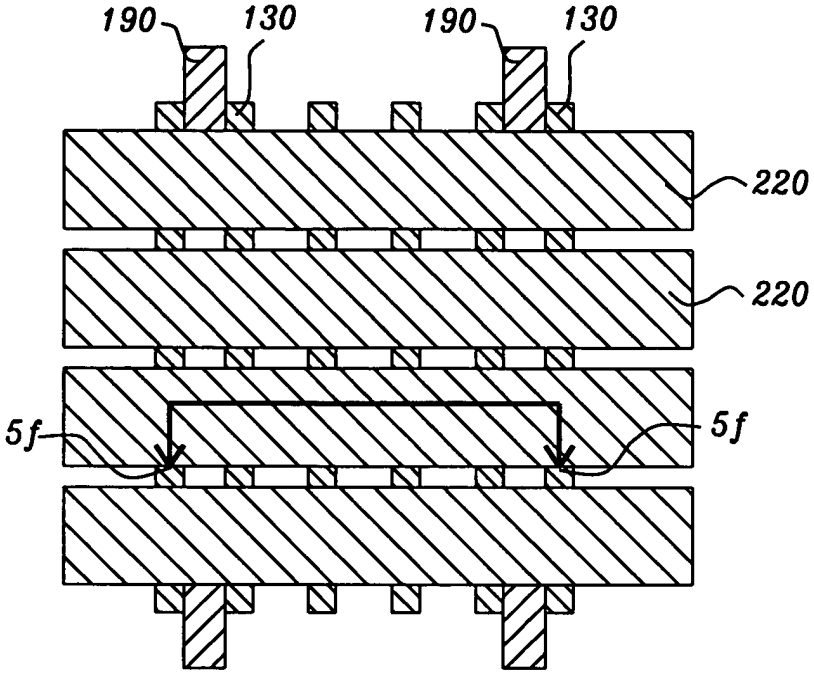


FIG. 4f

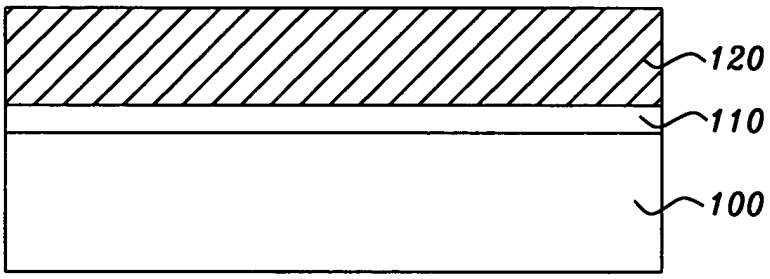
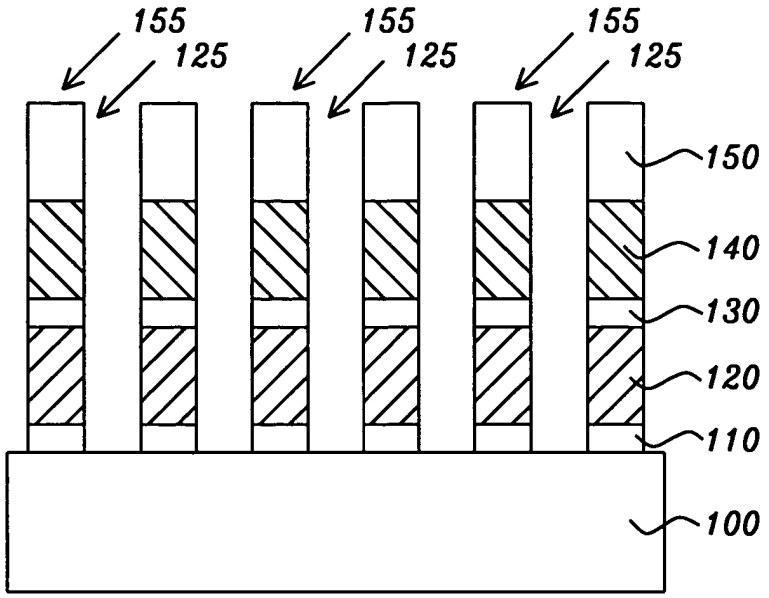


FIG. 5a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125
155
125
155
125
150
140
130
120
110
100

FIG. 5b

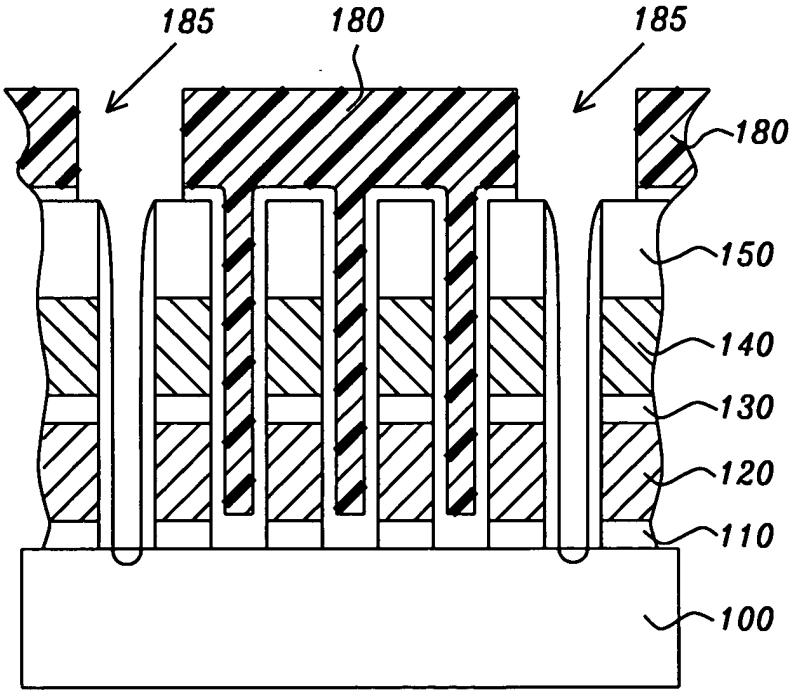
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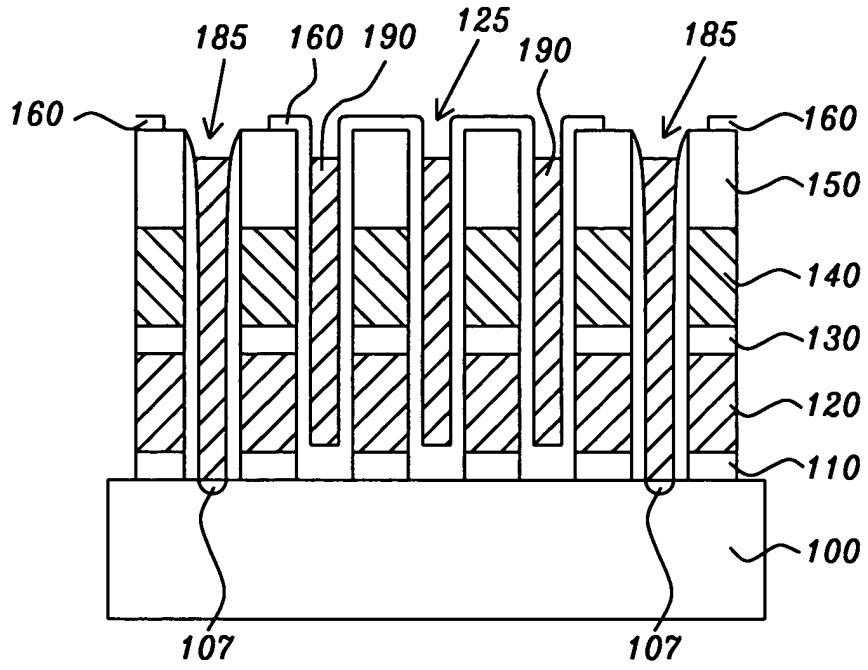
FIG. 5c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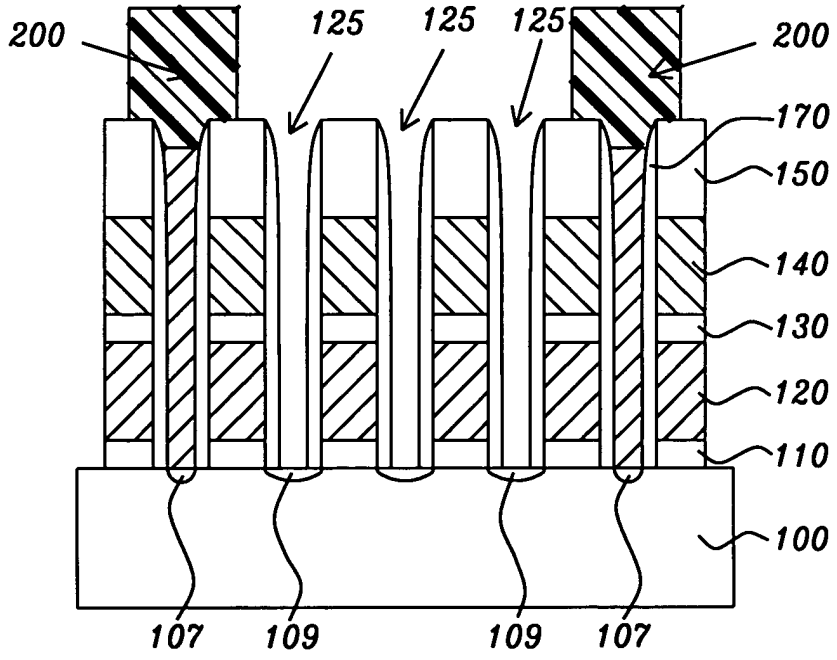
107
107

FIG. 5d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100
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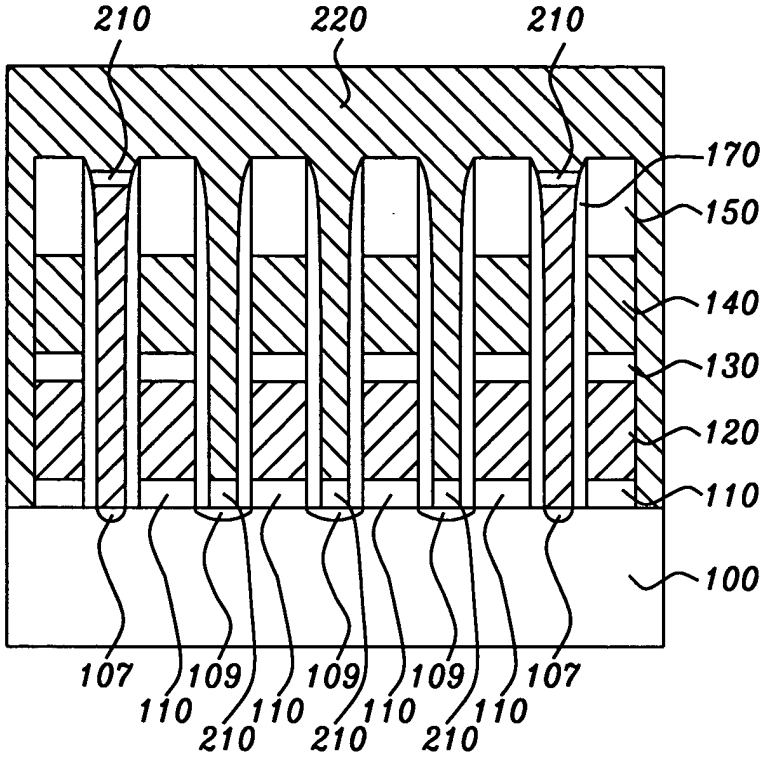
107

FIG. 5e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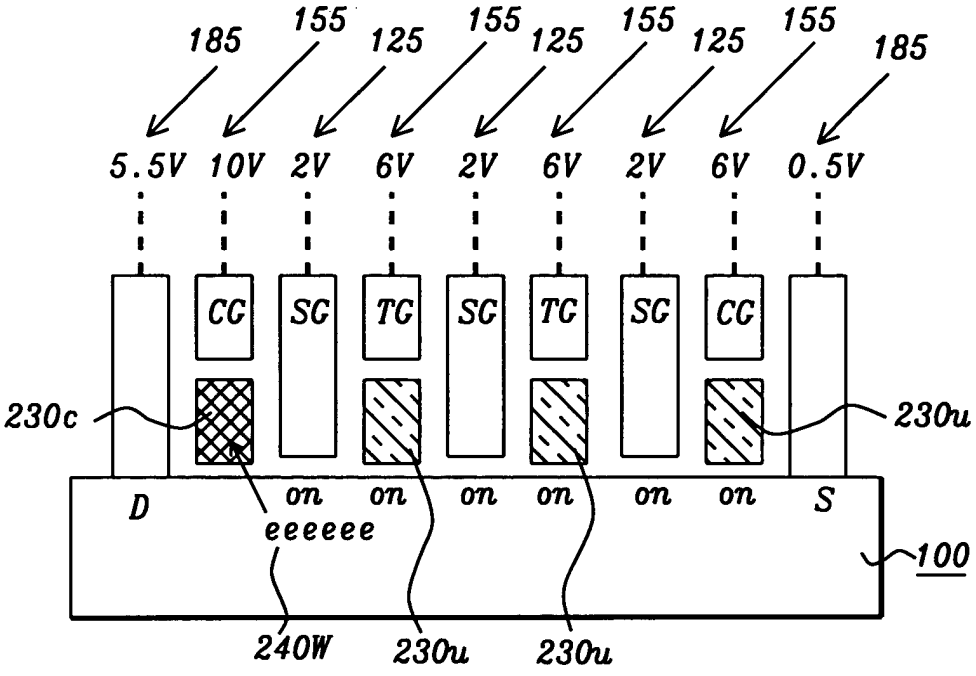
210
210

FIG. 5f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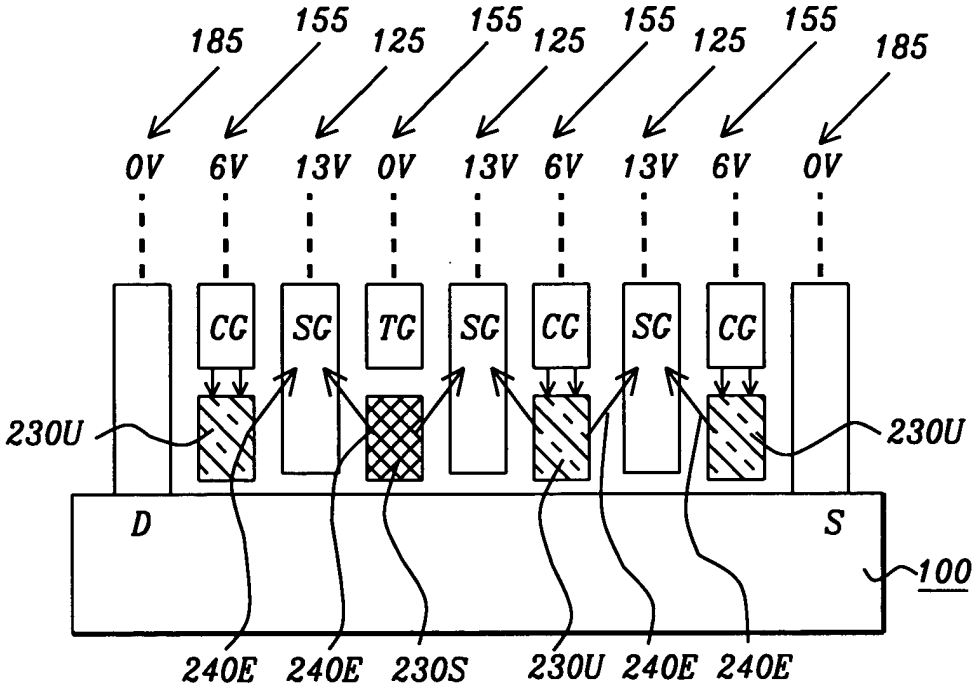
155
125
155
125
155
125
155
185
5.5V
10V
2V
6V
2V
6V
2V
6V
0.5V
CG
SG
TG
SG
TG
SG
CG
230c
230u
D
on
on
on
on
on
on
S
eeeeee
100
240W
230u
230u

FIG. 6a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155
125
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125
155
185
0V
6V
13V
0V
13V
6V
13V
6V
0V
CG
SG
TG
SG
CG
SG
CG
230U
230U
D
S
100
240E
240E
230S
230U
240E
240E

FIG. 6b

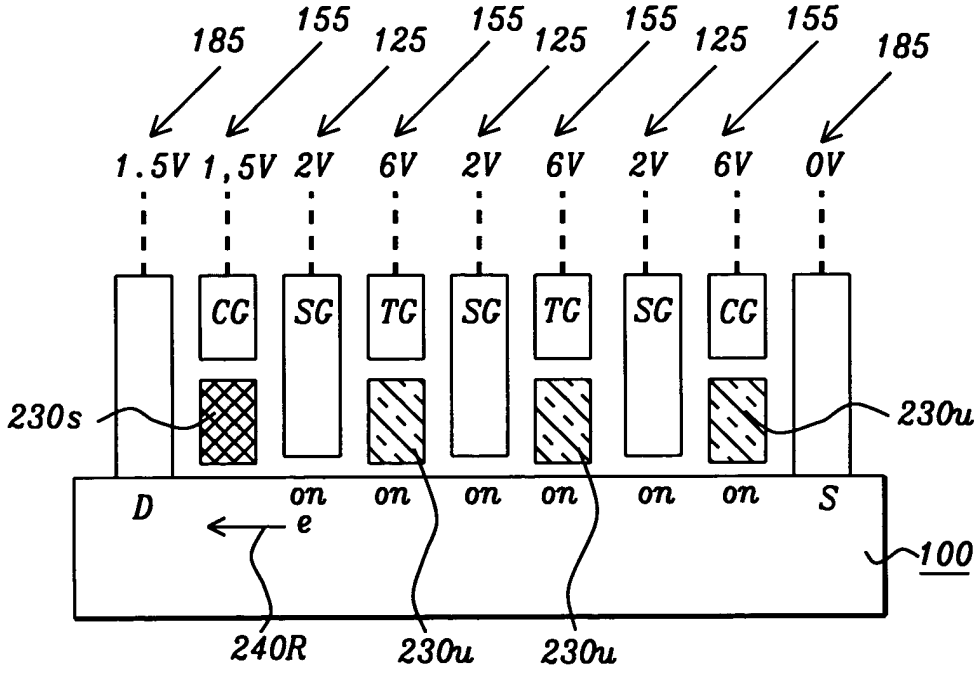
185
155
125
155
125
155
125
155
185
1.5V
1,5V
2V
6V
2V
6V
2V
6V
0V
CG
SG
TG
SG
TG
SG
CG
230s
230u
D
on
on
on
on
on
on
S
e
100
240R
230u
230u

FIG. 6c

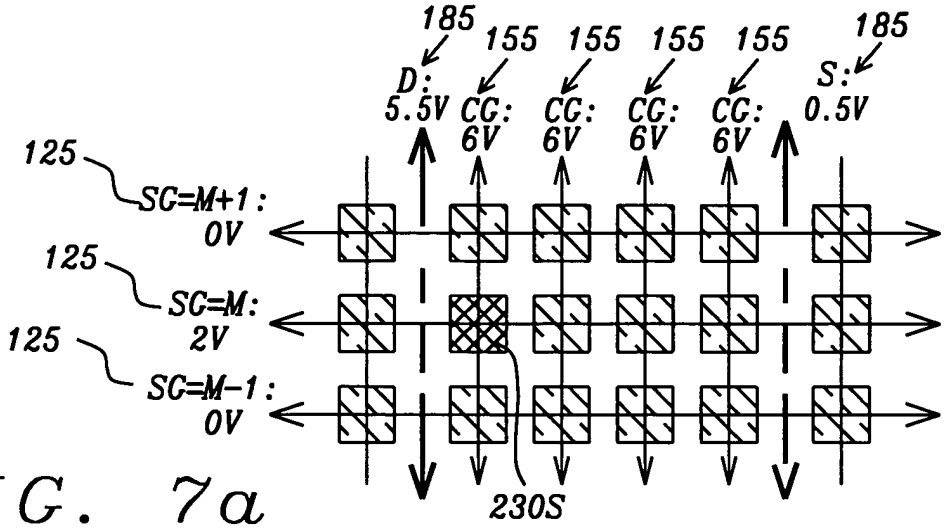

FIG. 7a

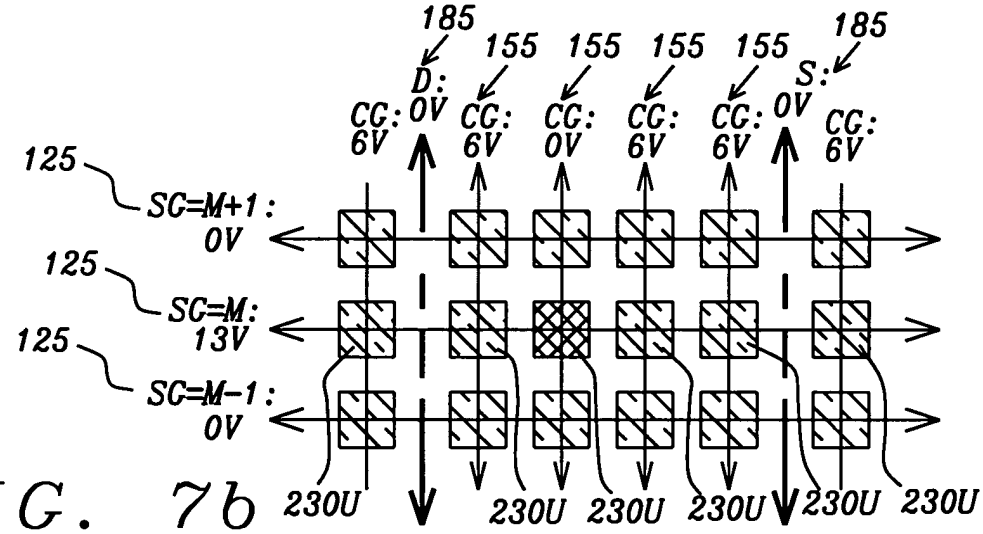

FIG. 7b

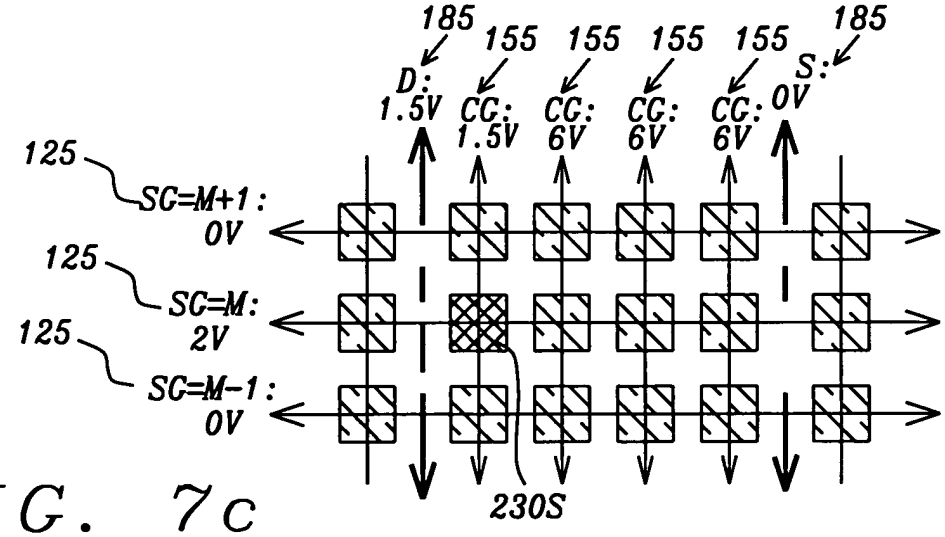

FIG. 7c